

In Place of FORM PTO-1449 (Modified)

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

Serial No. _____
Applicant: McBrearty et al.
Filing Date: _____
Group: _____
Atty. Docket No. AUS920030733US1

Reference Designation

U. S. PATENT DOCUMENTS

| Examiner Initial | Document Number | Date | Name | Class | Sub-class | Filing Date if Appropriate |
|------------------|-----------------------|------------|---|-------|-----------|----------------------------|
| BB | AA US 6,601,135 | 7/29/2003 | No-Integrity Logical Volume Management Method and System | 711 | 112 | 11/16/2000 |
| | AB US 2003/0097536 A1 | 5/22/2003 | System and Method for Physical Memory Allocations in Advanced Operating Systems | 711 | 170 | 11/7/2001 |
| | AC US 2003/0005257A1 | 1/2/2003 | Memory Table and Memory Manager For Use in Managing Memory | 711 | 205 | 6/28/2001 |
| | AD US 6,233,666 | 5/14/2001 | Deferred Disk Drive Space Allocation for Virtual Memory Pages with Management of Disk Address Recording in Multi-page Tables Without External Process Interrupts for Table for Input/Output to Memory | 711 | 203 | 9/17/1998 |
| | AE US 6,119,214 | 9/12/2000 | Method for Allocation of Address Space in a Virtual Memory System | 711 | 206 | 4/25/1994 |
| | AF US 5,940,868 | 8/17/1999 | Large Memory Allocation Method and Apparatus | 711 | 203 | 7/18/1997 |
| | AG US 5,860,144 | 1/12/1999 | Addressing Method and System for Providing Access of a Very Large Size Physical Memory Buffer to a Number of Processes | 711 | 206 | 8/9/1996 |
| | AH US 5,835,925 | 11/10/1998 | Using External Registers to Extend Memory Reference Capabilities of a Microprocessor | 711 | 2 | 3/13/1996 |
| BB | AI US 5,796,978 | 8/18/1998 | Data Processor Having an Address Translation Buffer | 395 | 416 | 9/7/1995 |

AB

Operable With Variable Page
Sizes

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|-----------|-----------------|------------|---|-----|-----|------------|
| AJ | US 5,721,858 | 2/24/1998 | Virtual Memory Mapping Method and System for Memory Management of Pools of Logical Partitions for BAT and TLB Entries in a Data Processing System | 395 | 413 | 12/12/1995 |
| AK | US 5,652,873 | 7/29/1997 | System and Method for Simulating a Contiguous Addressable Data Space | 395 | 500 | 5/17/1995 |
| AL | US 5,446,854 | 8/29/1995 | Virtual Memory Computer Apparatus and Address Translation Mechanism Employing Hashing Scheme and Page Frame Descriptor That Support Multiple Page Sizes | 395 | 401 | 10/20/1993 |
| AM | US 5,392,415 | 2/21/1995 | System for Grouping Non-Contiguous Pages Belonging to a Storage Object for Page Out | 395 | 425 | 12/15/1992 |
| AN | US 5,058,003 | 10/15/1991 | Virtual Storage Dynamic Address Translation Mechanism for Multiple-Sized Pages | 364 | 200 | 12/15/1988 |
| <i>MS</i> | AO US 4,730,249 | 3/8/1988 | Method to Operate on Large Segments of Data in a Virtual Memory Data Processing System | 364 | 200 | 1/16/1986 |

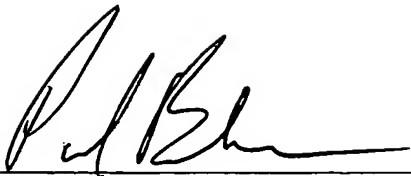
FOREIGN PATENT DOCUMENTS

| Examiner Initial | Document Number | Date | Country | Class | Subclass | Translation |
|------------------|-----------------|------|---------|-------|----------|-------------|
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

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Examiner:



Date Considered:

10/26/05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
